In the Claims:

Please amend claims 1, 8, 11, 14 and 15. Please cancel claims 4, 7, 9, 17 and 20-22. Please add new claims 23-26. The claims are as follows:

1. (Currently Amended) A ~~tunneling leakage current compensation~~ circuit, comprising:

~~a current mirror coupled to~~ a tunneling leakage monitor circuit, said tunneling leakage monitor circuit comprising a first PFET, a second PFET, a first NFET and a second NFET, sources of said first and second PFETS connected to a voltage source, gates of said first and second PFETs and said drain of said first PFET connected to a drain of said first NFET, a drain of said second PFET connected to a gate of said second NFET, sources of said first and second NFETs and a drain of said second NFET connected to ground;

a current mirror ~~coupled~~ connected to a gate of said first NFET ~~including a tunneling leakage monitoring device~~, said current mirror adapted to force a current of a predetermined value from said gate of said second NFET, through a gate dielectric layer of said second NFET, through said source and said drain of said second NFET to ground, ~~through said tunneling leakage device to a predetermined current value~~, said current ~~comprising only~~ consisting of tunneling leakage current; and

an input of a voltage buffer ~~coupled~~ connected to said ~~leakage monitor~~ gate of said second NFET, said voltage buffer adapted to generate an output voltage based on a voltage level developed across said ~~leakage monitoring device~~ gate dielectric layer of said second NFET when said current is at said predetermined current value.

2. (Original) The circuit of claim 1, wherein said current mirror includes an adjustable current source and means to adjust a current generated by said current source.

3. (Previously Presented) The circuit of claim 2, wherein said current source is a band gap current source and said means to adjust said current generated by said current source is a digital to analog converter.

4. (Canceled)

5. (Previously Presented) The circuit of claim 4, further including a fuse array, said fuse array adapted to apply input signals to inputs of said digital to analog converter based on a state of fuses in said fuse array or a field programmable gate array, said field programmable gate array adapted to apply input signals to inputs of said digital to analog converter based on a programming of said field programmable gate array.

6. (Original) The circuit of claim 1, further including a voltage regulator coupled to said voltage buffer, said voltage regulator adapted to supply a fixed voltage to a power distribution network of an integrated circuit chip based on said output voltage of said voltage buffer.

7. (Canceled)

8. (Currently Amended) A method of compensating for tunneling current leakage in an integrated circuit chip, the method comprising:

forcing a current of known value only through a dielectric layer of a tunneling current leakage monitor circuit ~~device~~ to provide a voltage signal, said tunneling leakage monitor circuit comprising a tunneling leakage monitor circuit, said tunneling leakage monitor circuit comprising a first PFET, a second PFET, a first NFET and a second NFET, sources of said first and second PFETS connected to a voltage source, gates of said first and second PFETs and said drain of said first PFET connected to a drain of said first NFET, a drain of said second PFET connected to a gate of said second NFET, sources of said first and second NFETs and a drain of said second NFET connected to ground; and

regulating an on-chip power supply of said integrated circuit chip based on said voltage signal.

9. (Canceled)

10. (Original) The method of claim 8, further including programming fuses or a field programmable gate array in order to set said value of said known current.

11. (Currently Amended) The method of claim 8, further including performing a [[burn-in]] test at a voltage level higher than a normal operating voltage level of said integrated circuit chip while forcing said current of known value through ~~a tunneling current leakage monitor device~~ a gate dielectric layer of said second NFET.

12. (Original) The method of claim 8, wherein said current of known value is selected to be about equal to the tunneling leakage current of a worst-case process integrated circuit chip.

13. (Original) The method of claim 8, further including lowering a voltage level of said on-chip power supply for a best-case process integrated circuit chip from a nominal value for a nominal-case process integrated circuit chip and raising said voltage level of said on-chip power supply for a worst-case process integrated circuit chip from said nominal value.

14. (Currently Amended) The method of claim 8, further including:

selecting a first value for said current of known value for burn-in ~~operation~~ testing of said integrated circuit that is higher than a second value for said current of known value for normal operation of said integrated circuit; and

determining a voltage level of a burn-in test power supply based on said first value.

15. (Currently Amended) A method of compensating for tunneling current leakage in an integrated circuit chip, the method comprising:

providing ~~a current mirror coupled to~~ a tunneling leakage monitor circuit, said tunneling leakage monitor circuit comprising a first PFET, a second PFET, a first NFET and a second NFET, sources of said first and second PFETS connected to a voltage source, gates of said first and second PFETs and said drain of said first PFET connected to a drain of said first NFET, a drain of said second PFET connected to a gate of said second NFET, sources of said first and second NFET's and a drain of said second NFET connected to ground;

providing a current mirror, said current mirror ~~coupled~~ connected to a gate of said first NFET ~~including a tunneling leakage monitoring device~~, said current mirror adapted to force a current of a predetermined value from said gate of said second NFET, through a gate dielectric

layer of said second NFET, through said source and said drain of said second NFET to ground, ~~through said tunneling leakage device to a predetermined current value~~, said current ~~comprising~~ ~~only~~ consisting of tunneling leakage current; and

providing a voltage buffer, an input of [[a]] said voltage buffer ~~coupled~~ connected to said ~~leakage monitor~~ gate of said second NFET, said voltage buffer adapted to generate an output voltage based on a voltage level developed across said ~~leakage monitoring device~~ gate dielectric layer of said second NFET when said current is at said predetermined current value.

16. (Previously Presented) The method of claim 15, wherein said current mirror includes a current source and a digital to analog converter.

17. (Canceled)

18. (Original) The method of claim 17, further including providing a fuse array, said fuse array for applying input signals to inputs of said digital to analog converter based on a state of fuses in said fuse array or providing a field programmable gate array, said field programmable gate array for applying input signals to inputs of said digital to analog converter based on a programming of said field programmable gate array.

19. (Original) The method of claim 15, further including providing a voltage regulator coupled to said voltage buffer, said voltage regulator for supplying a fixed voltage to a power distribution network of an integrated circuit chip based on said output voltage of said voltage buffer.

20 - 22 (Canceled)

23. (New) The circuit of claim 1, wherein said voltage buffer comprises a digital amplifier and a third PFET, an output of said digital amplifier connected to a gate of said third PFET, a source of said third PFET connected to said voltage source, a drain of said third PFET connected to an additional input of said digital amplifier and to an output of said voltage buffer.

24. (New) The circuit of claim 1, further including:

a voltage regulator connected to an output of said voltage buffer; and

a power distribution network of an integrated circuit chip connected to an output of said voltage regulator.

25. (New) The method of claim 15, wherein said voltage buffer comprises a digital amplifier and a third PFET, an output of said digital amplifier connected to a gate of said third PFET, a source of said third PFET connected to said voltage source, a drain of said third PFET connected to an additional input of said digital amplifier and to an output of said voltage buffer.

26. The method of claim 15, further including:

providing a voltage regulator connected to an output of said voltage buffer; and

providing a power distribution network of an integrated circuit chip connected to an output of said voltage regulator.